Modelling of Electronics Packaging and Developments in Heterogeneous Integration

Contact

Office of Continuing Education
Indian Institute of Technology Kharagpur,
Kharagpur – 721302
West Bengal, INDIA
Email: adeanoutr@iitkgp.ac.in

About IIT Kharagpur

History

First in the chain of IITs to be set up by the Government of India, Indian Institute of Technology, Kharagpur started in 1951 in the erstwhile Hijli Detention Camp. It has now blossomed into one of the finest technical institutions in the world. Spread over a sprawling campus of 2100 acres, it is largest and most diverse technical institution in the country offering programmes in Bachelors, Masters and Ph.D. levels in all disciplines of engineering, basic sciences, medical and life sciences, management, law and humanities.

Location

Situated about 120 km west of Kolkata, Kharagpur can be reached in about 2 hours by train from Howrah railway station of Kolkata or 3 hours by car from Kolkata Airport. Kharagpur is also connected by direct train services to most major cities of the country. The Institute is about 10 minutes drive (5 km) from the Kharagpur railway station. Private taxi, autorickshaw or cycle-rickshaw can be hired to reach the Institute.

Weather

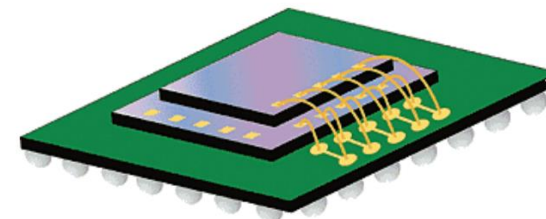
Winter (October to February) is moderate and pleasant (10 to 25 C) in Kharagpur. Summer (March to June) is hot (25 to 40 C) and sometimes humid. Rains are normally confined to the months of June to September.

Overview

Chiplets, advanced packaging, and heterogeneous integration are recent technologies in electronics packaging which are integrating electronics into all manner of products and applications, embedding electronics into every facet of our lives and making them ubiquitous in every engineering system.

We are facing an ever-increasing demand in the speed and amount of information we need to transmit, communicate and process. To meet this demand and compete in the international marketplace, we have to constantly seek methods to achieve early adoption of new and emerging technologies, improve quality and reliability, and reduce cost. It is now generally recognized that the performance and price of an electronic system are ultimately limited, not so much by advancements in new device and chip technology, but by our ability to package and manufacture these individual chips into modules, substrates, boards, sub-systems and systems.

Electronic packaging is one of the most critical topics that a practicing engineer in the electronics industry must know about. It is the science and technology that takes the VLSI microchip and transforms it into an usable system/product. The design of an electronic system requires engineering expertise from many different disciplines. In fact, cost, size, weight, manufacturability, quality, reliability, and even commercial success of electronic systems and products depend on holistic system design that require emphasis on mechanical design (based on the principles of mechanics and thermal transport), manufacturing and materials engineering, not just on electrical design.



Objectives of the Course

This course is designed to provide a basic knowledge of the technologies and processes required for the packaging and manufacturing of electronic products. The focus of the course will be on the mechanical, materials and manufacturing aspects which are often neglected in the design phase with potentially catastrophic consequences. Students will be exposed to the underlying scientific and technological knowledge-base needed to become proficient builders and users of electronic systems. Course topics will include fundamental principles for packaging active and passive electronic devices; design and testing of components, circuit boards, connectors, and assemblies; thermal, mechanical, electrical and multi-physics modelling; and reliability assessment methods.

Course Schedule and Methods

Dates: May 14, 2022
Duration: 5 hours

Eligibility

- Engineers, managers/executives and researchers responsible for building, using and sustaining electronic products.
- Researchers from R&D laboratories working on Electronic Packaging, Design and Manufacturing
- Graduate students and senior undergraduate students from reputed academic and technical institutions at all levels
- Faculty from reputed academic and technical institutions

The course does not have any pre-requisites and is designed to cater to an audience with diverse backgrounds.

Important Dates

Last date for receiving application: 11th May, 2022

Course Contents

1

Introduction to Electronic Packaging

- History of Electronic Packaging
- Function of Electronic Packaging
- Surface Mount Technology
- Microelectronics Packaging
- Power Electronics Packaging
- Challenges

Heterogeneous Integration

2

- System on Chip (SoC) vs System in Package (SiP)
- Chiplets & Heterogeneous Integration
- 2D, 2.5D and 3D IC Integration
- Materials for Advanced Packaging
- Additive Manufactured Electronics
- Advanced Interconnects

3

Design and Test

- Traditional Design Flows
- Physical Design
- Electrical and Thermal Design
- Mechanical Design
- Qualification Testing
- Failure Analysis and Reliability Testing

Modelling Tools

4

- Different Levels of Model Abstraction
- Circuit Simulators
- Finite Element Analysis
- Electrical Modelling
- Thermal Modelling
- Stress Analysis

5

- Chip-Package-System Interactions
- Multi-Physics Modelling & Optimisation
- Physics of Failure Reliability
- Digital Twins
- Case Studies

The Faculty

Prof. Christopher Bailey is Professor of Computational Mechanics and Director of the Computational Mechanics and Reliability Group at the University of Greenwich, UK. He has over 25 years professional experience in electronic packaging (both microelectronics and power electronics) with a particular focus on design tools and modelling for electrical, thermal and reliability assessments of electronic packaging. In the 2014 UK Research Excellence Framework, over 70% of Professors Bailey's research outputs and impact of his work was rated in the two highest categories of internationally excellent and world leading.

Professor Bailey is considered internationally to be a pioneer in the area of design tools and modelling for electronic packaging and systems. In 2009 his work received the Times Award of Outstanding Engineering Research Team, and his work in knowledge transfer to industry has received numerous awards including best knowledge transfer partnership in 2008. He has published over 300 papers in journals and professional conferences, and his work has received best paper prize at a number of conferences; the most recent being Fraunhofer Direct Digital Manufacturing Conference, Berlin, Germany, 2016.

Professor Bailey is also a regular invited keynote and short course presenter at international conferences. Apart from being an outstanding academic, Professor Bailey has consulted with over 40 companies worldwide providing both technical expertise and guidance as well technical expertise in expert witness work in the USA. Professor Bailey is also a co-investigator on the £18M UK Government multi-university research centre in power electronics where he is leading the cross-theme topic of design tools and modelling (*http://www.powerelectronics.ac.uk*).

Professor Bailey is also affiliated with the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society. From 2020-2021 he served as the society's president, and he is also leading on the co-design, modelling and simulation activities for the Heterogeneous Integration Technology roadmap which is sponsored by a number of IEEE societies as well as other professional societies such as ASME and SEMI.

Registration Fees

IITKharagpur students: INR 100 + GST

Students of other institutions: INR 250 + GST

Participants from Industry: INR 2000 + GST

Faculty from academic Institutions: INR 1000 + GST

Accommodation

Accommodation and food for participants can be arranged on separate payment basis.

Registration Link

Please register at:
https://erp.iitkgp.ac.in/CEP/courses.htm

Course Coordinator

Dr. Anandaroop Bhattacharya
Dept. of Mechanical Engineering
IIT Kharagpur
Kharagpur – 721302, India
Phone: +91 3222 - 282946
E-mail: anandaroop@mech.iitkgp.ac.in

NOTES

SHORT TERM COURSE

Modelling of Electronics Packaging and Developments in Heterogeneous Integration

14TH May, 2022