About IIT Kharagpur

Kharagpur-a dusty town tucked away in the eastern corner of India, famous until 1950 as home to the longest railway platform in the world - became the nursery where the seed of the IIT system was planted in 1951. IIT Kharagpur started its journey in the old Hijli Detention Camp in Eastern India, where some of the country's great freedom fighters toiled and sacrificed their lives for India's independence. Spurred by the success of IIT Kharagpur, four younger IITs sprouted around the country in the two following decades, and from these five came thousands of IITians, the brand ambassadors of modern India. It was the success of this one institution at Kharagpur that wrote India's technological odyssey.

The Institute takes pride in its relentless effort to provide the best platform for both education as well as research in the areas of science and technology, infrastructure designs, entrepreneurship, law, management, and medical science and technology. IITKGP is not just the place to study technology, it is the place where students are taught to dream about the future of technology and beam across disciplines, making differences enough to change the world.

Program Features/ Structure

Lectures – 50%

Hands-on modeling and analysis in MATLAB – 25%

Hands-on design in Cadence – 25%

Program Schedule and Venue

1 week, 9 – 14 September, 2019 (9:00AM – 6:00PM)

IIT Kharagpur,

Dept. of E&ECE

Program Fee

Scientists and Engineers from industry, Govt., or other institutions – ₹18,000 (Eighteen thousand) + GST @ 18% per participant

Accommodation

Accommodation and food will be provided to the participants at the campus Technology Guest House on chargeable basis. Accommodation charge is ₹1500/-per day for double occupancy plus 12% (GST) charges.

How to Apply

The course fee can be paid online through IIT Kharagpur web-portal by following the steps given below (candidates applying in a group can however pay their fees offline through demand draft drawn in favour of **'CEP-STC, IIT Kharagpur',** payable at **Kharagpur.**)

- Candidates paying online should apply by clicking "**APPLY for CEP Events"** under the **"EVENTS"** section in the Institute website **www.iitkgp.ac.in**.
- Click on **How to Apply** at the top the page. Follow the instructions given there for signing up & editing your profile. Scroll down to the course **Short Term Course on "Calibration Techniques for Pipelined ADCs"**
- Click on the **"Apply Now"** Button and follow point no. 1-6 mentioned in the instruction page available at the **How to Apply** link.

Deadline for receiving application: Sept. 05, 2019

Contact Us

Dr. Bibhudatta Sahoo
Dept. of E&ECE,
Indian Institute of Technology, Kharagpur
Phone:+91-3222-283518
Email: bsahoo@ece.iitkgp.ac.in
mishrasudha06@gmail.com

Short Term Course

Calibration Techniques for Pipelined ADCs

1-week
9-14 Sept. 2019

A Continuing Education Program of Indian Institute of Technology Kharagpur

Organized by
Department of Electronics and Electrical Communication Engineering

Indian Institute of Technology Kharagpur – 721 302

Overview

The alarming rate at which the transistor sizes have been shrinking in the past decade poses great challenges for analog and mixed-signal circuits that interface with real-world signals. However, this scaling trend has provided the IC industry with faster and cheaper transistors suitable for digital circuits.

The analog-to-digital interface is the performance bottleneck in most mixed-signal or communication systems. We have reached an inflection point in the design of these interfaces: the "analog" designer must now know much more than analog design. The modern analog designer needs to capitalize on the immense DSP capabilities available in the current low voltage-nanometer-CMOS technologies. Time has therefore come to use thousands of "digital" transistors as a workhorse for a handful of analog transistors, thus unleashing a new era of digitally calibrated analog-to-digital converters (ADCs).

This short-course begins with an introduction to the scaling trend in transistors and power dissipation trends of data converters. Design challenges of pipelined ADC in nanometer CMOS will be discussed followed by a discussion on strategies/methodologies for designing high-resolution, low-power, and high-speed pipelined ADC. The course will then comprehensively cover various ***analog*** and ***digital calibration*** techniques that have been developed over the last two-decades.

Program Objectives

Upon completing the course, the participant will be able to:

- Understand the challenges in pipelined ADC design in deeply scaled CMOS process.
- Understand design trade-offs to realize high-speed high-resolution pipelined ADCs in nanometer-CMOS.
- Understand various calibration techniques to mitigate and overcome analog component non-idealities.

Program Content

1. **Scaling trend and its impact on analog design**
    a. Trends in f_t.
    b. Trends in intrinsic gain.
    c. Variability.
2. **Pipelined ADC**
    a. Introduction to pipelined ADC
    b. Per stage resolution (1-bit/stage, 1.5-bit/stage, 2-bitstage, 2.5-bit/stage, etc.)
    c. Multiplying digital-to-analog converter (MDAC)
    d. Non-idealities in the MDAC and its impact on the ADC performance
    e. Impact of thermal noise
    f. Bootstrap switch
3. **Calibration Techniques for Pipelined ADCs**
    a. Analog Calibration Techniques
        i. Trimming
        ii. Capacitor Error Averaging
    b. Digital Foreground and background calibration techniques for the following:
        i. Gain error
        ii. Capacitor mismatch
        iii. Op amp nonlinearity
4. **Calibration Techniques for Time-Interleaved Pipelined ADCs**
    a. Inter-channel offset
    b. Inter-channel Gain error
    c. Inter-channel timing mismatch
    d. Inter-channel bandwidth mismatch
5. **Case Study:** Review of key papers incorporating various calibration techniques.

About the Faculty

Dr. Bibhudatta Sahoo

Bibhu Datta Sahoo received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 1998, the M.S.E.E. degree from the University of Minnesota, Minneapolis, MN, USA, in 2000, and the Ph.D.E.E. Degree from the University of California, Los Angeles in 2009. From 2000 to 2006, he was with DSP Microelectronics Group, Broadcom Corporation, Irvine, CA, where he designed analog and digital integrated circuits for signal-processing applications. From December 2008 to February 2010, he was with Maxlinear Inc., Carlsbad, CA, where he was involved in designing integrated circuits for CMOS TV tuners. From March 2010 to November 2010, he was a Post-Doctoral Researcher with the University of California, Los Angeles. From December 2010 to December 2011, he was an Assistant Professor with the Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, India. From January 2012 to May 2017, he was an Associate Professor with the Department of Electronics and Communication Engineering, Amrita University, Amritapuri, India. From January 2016 to May 2017 he was at University of Illinois at Urbana-Champaign on a sabbatical. Since August 2017 he has been Associate Professor at IIT Kharagpur. His research interests include analog and mixed signal circuit design, data converters, and signal processing.

He received the 2008 Analog Devices Outstanding Student Designer Award and was the co-recipient of the 2013 CICC Best Paper Award. He was the Associate Editor of IEEE Transactions on Circuits and Systems-II from Aug. 2014 to Dec. 2015.