VLSI Circuits & Company Compan



Summary:

An extensive summer-course with bottom-up approach, starting from re-cap of fundamentals, going all the way to essential building blocks and system level design. Hands-on simulation exercises follow in-depth theory modules, Covers both Analog and Digital Design concepts, Participants will be well equipped with essential fundamentals and skills related to design and verification of industry standard IPs. Participants can choose one or both of the modules- Analog Mixed Signal and Digital. Live as well as Recorded versions allow timing flexibility for students as well as working professionals.

Broad Topics:

Analog Mixed Signal

- Revisiting Basics of analog and digital circuit design- Devices and Circuits
- Design of Building Blocks: OPAMPS, Frontend Amplifiers, References. Switched Cap Circuits, Custom digital circuits, Data Converters,
- Applications: CMOS Image sensor readout, Audio sensor readout
- Power Management Units-LDO, DC-DC converters, High Speed I/O- SERDES

Digital

- Introduction to Digital Design Flow with examples.
- Design of Low Power Edge Computing Processor- from algorithm to RTL
- Introduction to In-Memory Computing for AI
- RTL for CNN accelerator
- System Design for a Biomedical Application

Simulation Modules:

Analog-LT-SPICE (Free Tool)/ Cadence

- Device Characterization, Basic Amplifiers, Biasing Circuits, References
- OPAMP-2-stage, folded cascode, output stages, Switched capacitor circuits
- Frontend Amplifier, LDO, ADC, Clocking and I/O blocks, System Simulation
- Image and audio acquisition system

Simulation Modules:

Digital - Vivado (Free Tool)

Basic Constructs, State Machines, Control and Data Paths, Registers and Memory access, Algorithm to RTL Architecture, Audio Classifier, CNN based Video Analysis unit

Eligibility:

- UG students in Electronics/Electrical Engineering, having covered basic circuits and signals processing courses
- PG/RS students in Electronics/Electrical Engineering, with specialization in VLSI
- Working Professionals in the field of VLSI

Timing & Schedule:

Dec 2025 - Feb 2026

Lecture Hours per week: 15

Timing- Live -5PM to 7PM, recording accessible, doubt clearing and interaction sessions

Weekly Quizzes, Simulation Modules with online demonstrations

Platform: K-Tech

Program Information :

Program Fees:

Students: INR 10k + 18% GST

Working Professionals: INR 30k + 18% GST

Program Coordinators:

Prof. Mrigank Sharad, Dr. Piya Sen

Program Information:

Email: mrigank@see.iitkgp.ac.in

Email: piya.sen@ktech.ltd

Phone No.: 8584979746

Web-site: www.ktech.click

