AI-Enabled VLSI Design

Executive Post Graduate Certification | IIT Kharagpur

8 MONTHS LIVE

DURATION & FORMAT	CADENCE ACCESS	CREDENTIAL	INDUSTRY PARTNER
32 Wks | Live Online	100 Hours Dedicated	IIT KGP Exec Alumni	Futurense.uni

Program Overview

The Executive PG Certification in AI-Enabled VLSI Design by IIT Kharagpur is an 8-month, 100% live online program engineered to bridge the gap between traditional simulation-only knowledge and production-ready silicon design. The curriculum focuses on architectural system design, Low-Power (UPF) strategies, Cadence signoff-grade EDA flows, and AI-driven Design Space Exploration (DSE) to prepare engineers for modern semiconductor demands.

Core Program Pillars & USPs

High-Fidelity Fusion Flow

Direct exposure to Vivado and Cadence toolchains (Genus, Innovus, Tempus, Voltus) mirroring real-world ASIC design and physical implementation.

Power-First Philosophy

Deep-dive into Low-Power RTL, UPF specifications, multi-voltage domains, and production-ready clock gating architectures.

AI-Integrated EDA Optimization

Utilize machine learning and AI algorithms for automated timing closure, floorplan prediction, and multi-knob Design Space Exploration (DSE).

Evidence-First Pedagogy

Build a verifiable candidate "Evidence Pack" containing design waveforms, timing/power logs, and Quality of Results (QoR) reports.

Traditional VLSI vs. IITKGP Fusion Flow

Feature	Traditional VLSI Courses	IITKGP AI-Enabled VLSI Flow
Verification	Local / Basic Simulation Only	Hyperscale & Signoff-Grade Verification
Design Focus	Standard RTL Coding	Power-Aware Architecture (UPF, Clock Gating)
Tooling & AI	Single-tool / No AI	Cadence Suite + AI-Assisted DSE & Timing Loop
Portfolio	Theoretical Code Projects	Silicon Evidence-Packs (Logs, DRC/LVS, QoR)

Program Faculty

Prof. Mrigank Sharad
Program Director | RM School of Engg. Entrepreneurship

Prof. Indrajit Chakrabarti
Professor | Dept. of E&ECE, IIT Kharagpur

Prof. Amit Kumar Dutta
Associate Professor | GS Sanyal School of Telecom

Curriculum Roadmap (32 Weeks)

Module	Topic Focus	Core Curriculum & Hands-on Tools
Mod 1–3 (W 1-10)	RTL, FSM & Datapath	Verilog modeling, combinational/sequential logic, FSM design, RAM/FIFO design, fixed-point DSP arithmetic, Vivado flow literacy.
Mod 4–5 (W 11-16)	Low-Power & Synthesis	Power types, 6 key low-power levers, clock gating, Cadence Genus synthesis, STA with Tempus, SDC constraints, TCL scripting.
Mod 6–8 (W 16-22)	Physical Design Baseline	Capstone spec plan, Cadence Innovus P&R, floorplanning, power grid planning, placement congestion mitigation, CTS overview.
Mod 9–10 (W 23-30)	Signoff & AI Optimization	RTL-to-GDSII flow, DRC/LVS physical verification, UPF power intent, Voltus/Joules power analysis, ML-based DSE, AI ECO tuning.
Mod 11–12 (W 31-32)	Portfolio & Showcase	Portfolio curation, interview readiness for RTL/PD/AI-EDA, capstone final showcase, commercial decision memo defense.

Industry Capstone Projects

01. Audio Processing NN
Hardware FFT/MFCC audio feature extraction paired with quantized NN classifier for wake-word/edge AI.

02. Tiny YOLO Accelerator
Streamlined CNN accelerator with MAC array design, INT8 quantization, and memory bandwidth tuning for edge vision.

03. ADAS Perception Hardware
Optical flow computation engine & real-time perception accelerator for autonomous vehicle vision systems.

Target Roles & Salaries

- **Low-Power Design Engineer:** ₹12 – 30 LPA
- **SoC / ASIC Design Engineer:** ₹10 – 35 LPA
- **Physical Design Engineer:** ₹8 – 25 LPA
- **VLSI / RTL Design Engineer:** ₹8 – 22 LPA
- **FPGA Design Engineer:** ₹8 – 20 LPA

Eligibility & Admission

- **Qualification:** B.Tech/B.E (4th Year / Graduate) or M.Tech in ECE, EE, VLSI, CS, IT, Physics/Electronics.
- **Min. Marks:** 50% aggregate or equivalent CGPA.
- **Process:** Online Application → Screening → Entrance Exam → Enrollment.
- **Fee:** ₹1.25 Lakhs + 18% GST (EMI options available).

Campus Immersion & Credentialing:
Includes a **2-Day In-Person Campus Immersion** at IIT Kharagpur for networking, faculty interaction, and lab visits. Upon completion, participants receive an official Certificate from IIT Kharagpur and gain **Executive Alumni Status**.