Course Title: Quality and Reliability assessment of Advanced microelectronics Packaging

Instructors: Shubhada Sahasrabudhe, Shalabh Tandon | QuRIuS LLC

Course abstract:

Semiconductor packaging is back in limelight to meet the functionality and high-performance needs of the AI market. Given the immense cost of these AI products platforms, an important and differentiating factor for a successful packaging technology supplier is offering stellar quality and reliability (Q&R) to preserve the value of the expensive silicon devices integrated heterogeneously which in turn reduces the overall cost of ownership. One way to guarantee high quality and reliability of new technologies is to overdesign but that can be expensive. Under- designing packages from a quality perspective may be cheaper, however, it will trigger premature failure, leading to higher ownership costs and frustration for customers. Striking the balance between market demand and technology capability requires drawing from experience (data), judicious use of simulations, augmenting with empirical data and more importantly, engineering rigor to make the optimum technology decisions.

This course presents a methodology for both optimum approach to delivering and quantifying, Q&R figures of merit (DPM, %fail) for complex heterogenous integration products. It will prepare the audience to tackle Q&R challenges by providing a blueprint that aids in proving that the technology capabilities can meet the market demands. The participants will experience the concepts through hands-on exercises throughout the course.

Course structure:

6 modules x 2 hours each

Who should attend?

Undergraduate/ Graduate students aspiring to gain knowledge in microelectronics packaging. Engineers involved in design, material selection, process development, certification of packaging technologies and customer technical support.

Course evaluation approach:

Quizzes, class exercises for every module,end of the course evaluation (MCQ)

Module Details

Module1-Electronics industry roadmap and technology trends [2 hours]

- Historical evolutionof components used in microelectronics products (transistors and packages)
- Integration of attendant ingredients that has brought about advanced package evolution.
- Overview of advanced packaging architectures (2.5D/3D) for emerging AI and general computing needs to enable low-latency, high-bandwidth, highly integrated systems.
- Prosand consofchipletsintegration (integrationchallenges, yield,cost, reliability).

Module 2 - Fundamental concepts of quality and reliability (Q&R) [2 hours]

- Definitionsand distinctions betweenQ and R
- Cost impact of failures and why it matters (scrap, rework, field returns, brand).
- Bathtub curve and failure regimes (early life, useful life, wear-out).
- Mapping of customer expectations- performance, quality, safety, regulatory, security and other requirements.
- Goalsetting (targetfailurerates,DPM,lifetimes)anduse conditionsaspart ofproductdefinition.

Module 3 - Q&R Considerations during Product Lifecycle Management (PLM) & Qualification Philosophy [2 hours]

- Class Quiz Details of PLM flow: early exploration / concept → design & feasibility → validation → ramp → mass
- production → field deployment and monitoring. Overview of how quality/reliability play a role at every step and what Q&R metrics are critical throughout. Challenges and impact across product life cycle with heterogeneous integration, diversity of materials, miniaturization and aggressive form factors, thermal/power
- challenges, harsh and diverse use environments (e.g., data centers in space). The philosophy of qualification: It's not just passing a JEDEC table but demonstrating that DPM goals and lifetime expectations are met for the intended application. Standards Based Qualification vs.
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  KnowledgeBased Qualification.

Module 4 – Microelectronics Packaging Reliability evaluation methodology / process – Part I [2 hours]

- Overview of a systematic 8 step framework used formicroelectronicsreliabilityevaluation.
- Deep dive discussion into the first 4 steps of the evaluation methodology
  - Use conditions (mission profile, environmental and operational conditions).
  - Stress conditions (accelerated test conditions).
  - Failure mechanisms (what can fail and how).
  - Failure analysis tools/infrastructure.
- ClassQuiz

Module 5 - Microelectronics Packaging Reliability evaluation methodology / process – Part II [2 hours]

- Class Exercise
- Deep dive discussion into the remaining 4 steps of the evaluation methodology
  - Life distributions and statistical analysis (Weibull, lognormal, etc.).
  - Acceleration factor / reliability models (e.g., Arrhenius, Eyring, voltage acceleration).
  - Use-condition reliability / DPM

- Comparison against goals and decision-making.

Module 6 - Design for Reliability (DFR), Manufacturing for Reliability (MfR) & Product Health Management [2 hours]

- DFR: building in reliability via design rules, modeling, safe operating areas, margining, etc.
- MfR: process controls, monitors, SPC, BIR (Building-In Reliability).
- Introduction to field health monitoring, telemetry, and product health management.
- Introduction to Critical Issue Management

Module 7 (Optional) – Office hours/ More class exercises [2 hours]

Instructor biographies:

Shalabh Tandon | LinkedIn | shalabh@quriusllc.com

Shalabh Tandon is a versatile and adaptive leader with expertise in semiconductor Quality and Reliability (Q&R), product development, behavior of polymers and high-volume manufacturing. With a PhD in Polymer Science and Engineering, he has led complex technical initiatives, managed critical issue resolution across products with functional, security, and supply chain implications. His ability to balance ambiguity and risk has positioned him as a key influencer among senior executives, technical fellows, and customer stakeholders.

Shubhada Sahasrabudhe | LinkedIn | shubhada@quriusllc.com

Shubhada Sahasrabudhe is a dynamic and impact-driven senior technical leader with a distinguished career in semiconductor Quality and Reliability (Q&R). With a strong background in product quality, innovation, and technology development, she has played a pivotal role in enhancing industry-wide quality strategies and fostering collaborations with major Data Center Companies. Her expertise spans quality modeling, testing methodologies, and customer quality experience, making her an invaluable asset in driving technological and business innovation.

Indian Institute of Technology, Kharagpur, India

Quality and Reliability Assessment of Advanced Microelectronics Packaging

ONLINE Short-Term Course

Course Date and Time (IST):

Module 1:	Mar 12, 2026	7:00 – 9:00 pm
Module 2:	Mar 14, 2026	9:00 – 11:00 am
Module 3:	Mar 26, 2026	7:00 – 9:00 pm
Module 4:	Mar 28, 2026	9:00 – 11:00 am
Module 5:	Apr 02, 2026	7:00 – 9:00 pm
Module 6:	Apr 04, 2026	9:00 – 11:00 am

Mode: **ONLINE** *(link to be shared)*

Registration Fee

Faculty from academia	**INR 5,000/- + GST**
Govt. of India research organisations	**INR 7,000/- + GST**
Industry professionals (including research labs)	**INR 10,000/- + GST**
Students *(except ME60006 Spring 2026)*	**INR 1,500/- + GST**
Students of ME60006 course, IIT Kharagpur in Spring 2026	**NIL**