

VLSI Circuits and Systems –Learn by Doing

Indian Institute of Technology Kharagpur

Summary:

An extensive summer-course with bottom-up approach, starting from re-cap of fundamentals, going all the way to essential building blocks and system level design. Hands-on simulation exercises follow in-depth theory modules; Covers both Analog and Digital Design concepts; Participants will be well equipped with essential fundamentals and skills related to design and verification of industry standard IPs. Participants can choose one or both of the modules- Analog Mixed Signal and Digital. Live as well as Recorded versions allow timing flexibility for students as well as working professionals.



Broad Topics

Analog Mixed Signal

- Revisiting Basics of analog and digital circuit design- Devices and Circuits
- Design of Building Blocks: OPAMPS, Frontend Amplifiers, References. Switched Cap Circuits, Custom digital circuits, Data Converters
- Power Management Units-LDO, DC-DC converters, High Speed I/O- SERDES

Digital

- Introduction to Digital Design Flow with examples.
- Design of Low Power Edge Computing Processor- from algorithm to RTL
- Introduction to In-Memory Computing for AI
- ARM Core Integration for SoC
- System Design for a Biomedical Application

Eligibility:

- UG students in Electronics/Electrical Engineering, having covered basic circuits and signals processing courses
- PG/RS students in Electronics/Electrical Engineering, with specialization in VLSI
- Working Professionals in the field of VLSI

Program Fees:

Students- INR 5k ; Working Professionals : INR 10k,

Program Coordinators- Prof. Mrigank Sharad, Prof. Amit K. Dutta Contact: mrigank@see.iitkgp.ac.in

Simulation Modules:

Analog-LT-SPICE (free tool)/ Cadence

- Device Characterization, Basic Amplifiers, Biasing Circuits, References
- OPAMP-2-stage, folded cascode, output stages, Switched capacitor circuits,
- Frontend Amplifier, LDO, ADC, Clocking and I/O blocks, System Simulation

Digital -Icarus (free tool)

Basic Constructs, State Machines, Control and Data Paths, Registers and Memory access, Deep Neural Network Architecture, ARM Core Integration

Timing and Schedule:

May 20- July 20

Lecture Hours per week: 15

Timing- Live -5PM to 7PM, recording accessible, doubt clearing and interaction sessions

Weekly Quizzes, Simulation Modules with online demonstrations
Platform- Gmeet + Youtube

Application Deadline : May 18th

Application Link