About IIT Kharagpur

Kharagpur - a dusty town tucked away in the eastern corner of India, famous until 1950 as home to the longest railway platform in the world - became the nursery where the seed of the IIT system was planted in 1951. IIT Kharagpur started its journey in the old Hijli Detention Camp in Eastern India, where some of the country's great freedom fighters toiled and sacrificed their lives for India's independence. Spurred by the success of IIT Kharagpur, four younger IITs sprouted around the country in the two following decades, and from these five came thousands of IITians, the brand ambassadors of modern India. It was the success of this one institution at Kharagpur that wrote India's technological odyssey.

The Institute takes pride in its relentless effort to provide the best platform for both education as well as research in the areas of science and technology, infrastructure designs, entrepreneurship, law, management and medical science and technology. IITKGP is not just the place to study technology, it is the place where students are taught to dream about the future of technology and beam across disciplines, making differences enough to change the world.

Program Features/Structure

Classroom lectures – **60%**

Numerical Problem Solving – **10%**

Hands-on design using Cadence **30%**

Program Schedule and Venue

5 days, 20 – 24 July 2020
(9:00 AM – 6:00 PM)

IIT Kharagpur – Department of Electronics and Electrical Communication Engineering

Program Fee

Nil for TEQIP-III sponsored participants

For others :
INR 15000/- + GST 18% (for teachers and others)
INR 10000/- + GST 18% (for outside students)
INR 20000/- + GST 18%
(for industry and R&D participants)

Who will benefit (Eligibility)

For TEQIP-III Institutes: Only faculty participants.
For others:
Teachers from Colleges/ Institutions/Universities.
Scientific Officers/Instructors/ Technical Assistants/Research Scholars/Under Graduate and Post Graduate Students/ Participants from Industries.

Last day of Registration

13th Nov. 2020

Accommodation

Accommodation will be provided to the TEQIP-III sponsored participants at the Campus Guesthouse. For other participants, the same will be provided on chargeable basis as per rules.

How to Apply

Use the link: **https://erp.iitkgp.ac.in/CEP/courses.htm** to apply ONLINE.

Signup → Login → Profile Fillup → Choose a Program → Apply Now

Payment if applicable is to be done **ONLINE** after being short listed for the program.

Contact Us

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NPIU

TEQIP-KIT

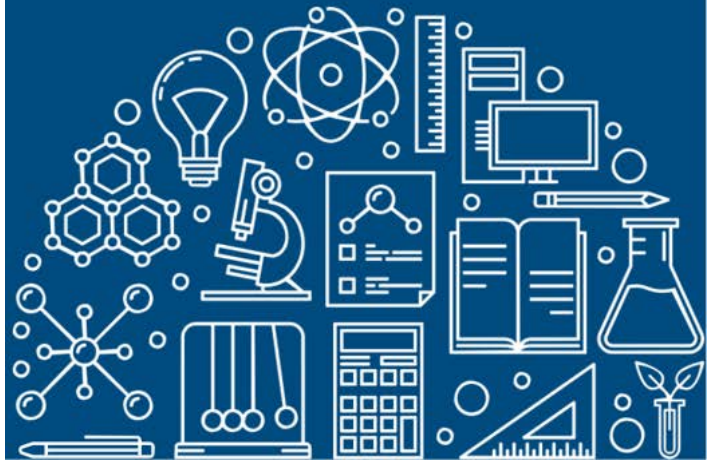
NPIU - A Unit of MHRD, Govt of India for Implementation of World Bank Assisted Projects in Technical Education

Indian Institute of Technology Kharagpur

Design of Analog Integrated Circuits in Nanometer CMOS

5 days

23-27 November 2020



Introduction/Overview

Primary focus of this course is to introduce design of analog and mixed signal circuits in nanometer CMOS and provide hands on experience in designing analog circuits using state-of-the art EDA tools like Cadence . A couple of Case-Study will also be taken up so that the participants get to apply the knowledge gained to real world applications.

Program Objectives

Nanometer CMOS analog and mixed-signal design differs significantly from conventional CMOS design because of the low intrinsic device gain, small headroom, higher noise, and larger variability. This program aims at introducing conventional CMOS analog design and methods to adapt those conventional techniques to realize reliable analog front-ends in nanometer CMOS. A couple of case-studies would also be discussed to bridge the gap between transistor level design and analog-subsystem design to meet certain system requirements. Layout techniques will also be discussed and the participants will be given a quick walk-through from **Schematic-to-GDS**, thus facilitating them a tape-out experience.

What you will learn

Program Content

Short-Channel Effects

Impact of Scaling

Single-Stage Amplifiers

Current Sources

Differential Amplifiers

Noise in Transistors

Feedback and Stability

Common Mode Feedback Circuit

Bandgap and Precision Circuits

Case Study I: Low Dropout Regulator (LDO)

Case Study II: Design of Signal Conditioning Circuit

Hands-on Design Using Cadence:

Single Stage Amplifier

Current Source

Noise Analysis

Two-stage fully differential op amp with CMFB

LDO Design

Chopper Amplifier Design

Layout techniques

About the Faculty

Dr. Bibhudatta Sahoo

Bibhu Datta Sahoo received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 1998, the M.S.E.E. degree from the University of Minnesota, Minneapolis, MN, USA, in 2000, and the Ph.D.E.E. Degree from the University of California, Los Angeles in 2009. From 2000 to 2006, he was with DSP Microelectronics Group, Broadcom Corporation, Irvine, CA, where he designed analog and digital integrated circuits for signal-processing applications. From December 2008 to February 2010, he was with Maxlinear Inc., Carlsbad, CA, where he was involved in designing integrated circuits for CMOS TV tuners. From March 2010 to November 2010, he was a Post-Doctoral Researcher with the University of California, Los Angeles. From December 2010 to December 2011, he was an Assistant Professor with the Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur, India. From January 2012 to May 2017, he was an Associate Professor with the Department of Electronics and Communication Engineering, Amrita University, Amritapuri, India. From January 2016 to May 2017 he was at University of Illinois at Urbana-Champaign on a sabbatical. Since August 2017 he has been Associate Professor at IIT Kharagpur. His research interests include analog and mixed signal circuit design, data converters, and signal processing.

He received the 2008 Analog Devices Outstanding Student Designer Award and was the co-recipient of the 2013 CICC Best Paper Award. He was the Associate Editor of IEEE Transactions on Circuits and Systems-II from Aug. 2014 to Dec. 2015