

Short Term Course on Advanced DSP Design Techniques (FREE for teachers from TEQIP-III Colleges)



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(<http://www.addt.iitkgp.ac.in/>)

Coordinator

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Scope of the Course

The course aims at providing a comprehensive coverage of techniques for designing efficient VLSI architectures for DSP, especially for applications like IOT, machine learning and big data. Towards this, architectural optimization both at block level as well as at logic level will be considered. The key issues that will be taken up are as follows:

- ◆ Graphical Representation of DSP Algorithms
- ◆ Retiming for Throughput Maximization
- ◆ Pipelined and Parallel Filter Structures
- ◆ Bit Serial Digital Filters
- ◆ Distributed Arithmetic and Multiplierless Realization
- ◆ Redundant Arithmetic
- ◆ DSP Architectures: Datapath and Control
- ◆ Speed-Power-Area-Accuracy Tradeoff
- ◆ Synchronous vs. Asynch. Designs
- ◆ Memory Bandwidth Management
- ◆ DSP for Embedded Applications

The course also intends to have a few Lab sessions in order to demonstrate digital design flow on Field Programmable Gate Array (FPGA), where the following modules may be covered:

1. Behavioral and Structural Description for Design Representation and Design Entry.
2. Validation through Functional Simulation.
3. Partitioning, Placement and Routing.



4. Post-routing Simulation for Performance Analysis. FPGA Specific Structural Optimization with respect to Speed and Area.
- 6 Configuration Bit Stream Generation for Actual Implementation on FPGA

The course may be viewed as a consolidated form of a semester long, graduate course on VLSI DSP system/architecture design. Participants from academia may thus find the course to be useful to develop similar courses at their respective institutions. Alternatively, the course may also be used as a reference by industrial professionals interested in VLSI design of signal processing and communication systems. *The course assumes minimal prerequisites - an undergraduate level knowledge of digital circuit design and elementary DSP operations is sufficient for one to be able to attend the course.*

About the Speakers

Prof. Mrityunjoy Chakraborty obtained Bachelor of Engg. (1983), M.Tech. (1985) and Ph.D. (1994) from Jadavpur University, IIT Kanpur and IIT, Delhi respectively. He joined IIT, Kharagpur as a lecturer in 1994, where he presently holds the position of a full professor.

Prof. Chakraborty has held many invited, visiting positions in reputed universities abroad. He is currently an associate editor of the IEEE Transactions on Circuits and Systems, Part I (2004-2007, 2010-2011) and part II (2008-2009), as a guest editor of the EURASIP JASP and a TPC member for many important IEEE conferences. The teaching and research interests of Prof. Chakraborty are in digital and adaptive signal processing, VLSI signal processing, wavelets and DSP for wireless communications, in which he has guided several Ph.D. students and published extensively. Prof. Chakraborty is a fellow of the INAE.

Prof. Anindya Sundar Dhar obtained Bachelor of Engg. in Electronics and Telecomm.Engg. from Bengal Engg. College (1987), followed by M.Tech. (1989) and Ph.D. (1994) from IIT Kharagpur. He is presently a professor in Electronics and Electrical Communication Engg., with teaching and research interests in VLSI architecture design for real time signal processing and communication. Prof. Dhar is a key person in the various VLSI related activities in the institute and has been offering many challenging courses in this area over years, apart from carrying out guided, independent and sponsored research in the above areas.

About IIT, Kharagpur

The IIT is located at Kharagpur, an important railway town about 116 km west of Kolkata.



Kharagpur is well connected to almost all part of the country by train. There are frequent train services from Howrah railway station to Kharagpur. The institute is about 5 km away from Kharagpur station and can be reached by taxis, auto-rickshaws, cycle-rickshaws etc. IIT, Kharagpur is the oldest IIT in the country and is the first among equals in terms of diversity in curricular as well as extra-curricular activities.

Registration Fees

NO fee to be paid by teachers from TEQIP-III colleges towards registration, boarding and lodging. For others, the following rates apply:

- Rs.9,000.00 for teachers from universities/ colleges.
- Rs.6,000.00 for students/research scholars.
- Rs.15,000.00 for people from Industry, and R&D labs (DRDO, ISRO etc)

♦ Registration fee includes 18% GST, access to all lectures and lab sessions, course material and course banquet.

♦ Accommodation will be arranged on *payment basis* in institute guest houses (*subject to availability, on first-come-first-serve basis*)

Guest House Room Rents:

Technology Guest House:

D/B AC Rooms(Single occupancy) – Rs 1000.
D/B AC Rooms(Double occupancy) – Rs 750 (per person).

Visveswaraya Guest House:

D/B AC Rooms(Double occupancy) – Rs 300 (per person).
D/B Non AC Rooms(Double occupancy) – Rs 150 (per person).
3 & 4 Bedded Non AC Rooms – Rs. 150 (per person)

Sir Asutosh Mukherjee Guest House:

AC Rooms (Single Occupancy) – Rs. 500

How to Apply:

- **For Teachers and Students:** Interested candidates may please visit the webpage of IIT Kharagpur at <http://iitkgp.ac.in/>. At the bottom right, you will find “All Events”. Click on “[Apply for CE Events](#)” where you will find the link to apply for various courses. It will also provide a link for payment.
- **For Industry and Defense Research Labs.:** For profile creation, follow the above procedure. For payment of registration fees, either pay online as above, or, pay by sending a demand draft drawn in favor of ‘CEP-STC, IIT Kharagpur’, payable at Kharagpur. The draft may be sent to :

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